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Research Article

DEVICE DESIGN OF 3-NM NODE-COMPLEMENTARY-FIELD EFFECT TRANSISTOR (CFET)

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A B S T R A C T

With a common gate, this CFET vertically stacks n-type and p-type nanosheet MOSFETs. Here, the ideal CFET device dimensions are examined in order to improve the electrical properties and inverter performance. Performance is examined for a number of CFET vertical dimension factors, encompassing how many stacked channels there are, the vertical distance (Dnsh) between nanosheet channels, the distance (Dn/p) between MOS separations, and the channel thickness (Tnsh). The findings indicate that, in contrast to typical CMOS, CFETs may efficiently increase inverter performance without experiencing significant deterioration by reducing their Dnsh and Dn/p, even though doing so forces a harsh trade-off between various parameters due to other dimensional factors. Due to electrical coupling, the decrease in Dnsh and Dn/p in the case of electrical characteristics marginally but significantly raises Tmax and Rth. Thus, a key technique for the creation of sub-3-nm CFETs will be the lowering of Dnsh and Dn/p.

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INTRODUCTION

Conventional FinFETs, which have recently been scaled down to 5-nm nodes, have almost reached physical limits in reducing fin thickness [1]. Thus, to improve gate controllability, nanosheet FETs (NSHFETs) with gate-all around (GAA) structures have been actively developed for sub-3-nm nodes [1]–[3]. However, they will continue to face these down-scaling limitations in the future. Therefore, to reduce the number of tracks and layout area to reduce the device footprint, the International Roadmap for Devices and Systems (IRDS) expects that a 3-dimensional structure which stacks multiple NSHFETs vertically can be a strong candidate for future technology nodes [4]–[11]. Thus, one of the most promising devices with a 3-dimensional structure, (CFET), which stacks n-NSHFET and p-NSHFET vertically with a shared gate for CMOS inverter operation in one device, has recently been suggested by Intel, Applied Materials, IMEC, and NARLab [4]–[9]. In addition, in a recent study on CFET, it was demonstrated that CFET with NSHFET shows better inverter performance than CFET with FinFET [8]. Recently, NSHFET have been replacing FinFETs for logic devices because of higher inverter operation frequency (f). This is owed to the lower effective resistance (Reff) of NSHFETs due to better current drivability and gate controllability in the same footprint [1]. However, the large effective capacitance (Ceff) of NSHFETs disturbs additional improvement of f or power-product delay (PDP). Therefore, a decrement of Ceff is an important factor for improving inverter performances. Furthermore, the CFET, which stacks vertically stacked NSHFETs also faces performance degradation by high Ceff because of the additional height of metal via of the vertically stacked structure. Recent studies demonstrated that CFET shows the possibility for better Ceff compared with conventional CMOS with NSHFETs because of fringe electric field overlap triggered by the reduced distance between nMOS and pMOS with the vertically stacked structure [4], [10]. In addition, recent fabrication processes demonstrated by Intel reduced number of metal via by connecting the drain of the nMOS and pMOS with one piece of metal via. This could additionally decrease Ceff.

However, CFET has a much higher height of metal via compared with conventional CMOS because of the stacked structure of the nMOS and pMOS. Therefore, there is still a risk of the degradation of Ceff, and the careful design of CFET is required. Therefore, analyzing Ceff and Reff of the CFET by varying dimensions is required to evaluate f and PDP [3]. In addition, it has been reported that multi-gate transistors such as NSHFETs are vulnerable to the self-heating effect (SHE) because of their confined geometry, which triggers thermal reliability issues [12]–[19]. In particular, it is expected that the high height of CFET makes it difficult for heat to dissipate to the thermal ground. Thus, finding a way to alleviate the SHE in CFET by stacking nNSHFETs and pNSHFETs is important. However, there has been no qualitative analysis of the optimal design of CFETs based on both thermal characteristics and CMOS inverter performances for different dimensions.

For the first time, the device design guideline of the 3-nm node CFET is investigated from the perspective of thermal

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characteristics and CMOS inverter accomplishment with carefully calibrated 3-D TCAD. First, the CMOS inverter performances of Ceff, Reff, f , and PDP in the 3-nm node CFET are analyzed by varying the dimensions of the number of stacked channels (NnMOS, NpMOS), distance between the nanosheets (Dnsh), n/pMOS separation distances (Dn/p), nanosheet channel thickness (Tnsh), and nanosheet width (Wnsh). Moreover, the maximum lattice temperature (Tmax) and thermal resistance (Rth) is evaluated in terms of different dimensions. Finally, the impact of the device design on the inverter performance and thermal characteristics is analyzed from the perspective of down-scaling.

MODELING METHODOLOGY

The 3-nm node CFET was designed for the front-end-of line (FEOL) based on the high-performance specification. The structure of CFET was based on the experimental reference of Intel [9].Fig. 1 shows the schematics of the 3-nm node CFET. Fig. 2 shows a 3-D bird's eye view of the CFET. Fig. 3, 4, 5, and 6 show the cross-sectional view of the 3-nm node CFET and schematics with structural parameters.

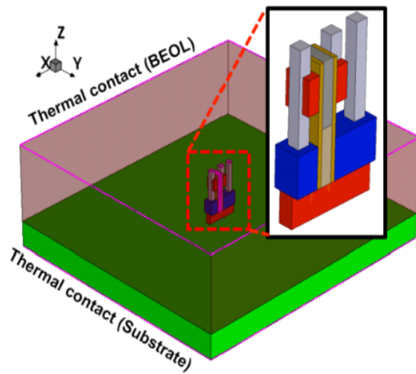

Fig. 1 3-nm node CFET

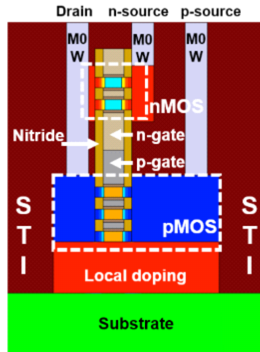

Fig. 2 CFET's cross-sectional view

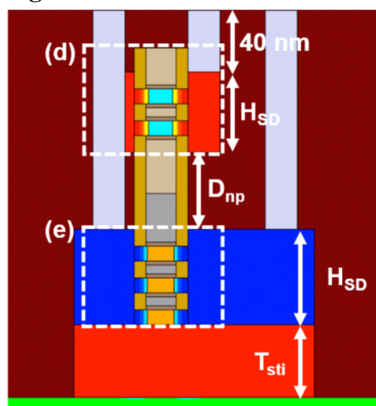

Fig. 3 Parameters of CFET in cross-sectional view

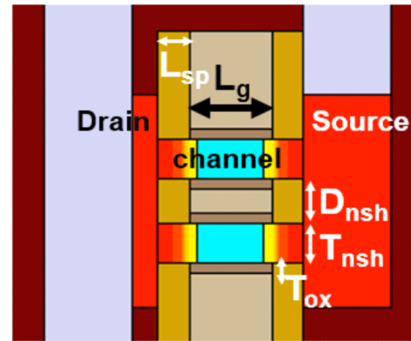

Fig. 4 CFET in cross-sectional view nMOS

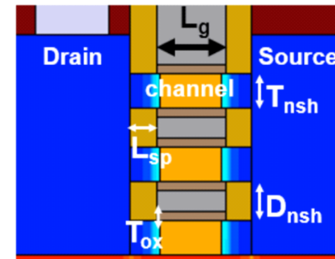

Fig. 5 parameters of CFET in cross-sectional view nMOS

Table 1 shows the structural parameters used in TCAD, and the reference values of each parameter are underlined.

Table 1 Structural parameters used for 3-nm complementary FET and reference values (underlined).

Quantity	Value	Description
L_{gate}	16 nm	Physical gate length
T_{oxide}	2 nm	Gate oxide thickness
N_{nMOS}	1 2 3 4	Number of stacked n-channel
N_{pMOS}	2 3 4 5	Number of stacked p-channel
W_{nsh}	15, 17.5, 20, 22.5, 25 nm	Nanosheet channel width
T_{nsh}	6, 7, 8, 9, 10 nm	Nanosheet channel thickness
D_{nsh}	7, 8, 9, 10, 11 nm	Distance between nanosheets
$D_{n/p}$	20, 30, 40, 50, 60, 70 nm	n/pMOS separation
$L_{S/D}$	10 nm	Source/drain (S/D) length
L_{spacer}	6 nm	Spacer length
$N_{it.nMOS}$	5×10^{12} cm^{-3} (Acceptor)	Interface trap conc. of nMOS
$N_{it.pMOS}$	1×10^{12} cm^{-3} (Donor)	Interface trap conc. of pMOS
Quantity	Doping concentration	Description
$N_{S/D}$ (nMOS)	1×10^{21} cm^{-3}	S/D doping concentration
$N_{S/D}$ (pMOS)	1×10^{21} cm^{-3}	S/D doping concentration
N_{sub} (nMOS)	1×10^{18} cm^{-3}	Substrate doping concentration
N_{sub} (pMOS)	1×10^{19} cm^{-3}	Substrate doping concentration
N_{Local}	1×10^{19} cm^{-3}	Local doping concentration

For CFET, nMOS-on-pMOS structure is assumed based on [9]. The physical gate length (Lg) was set as 16 nm. For the gate oxide, 2-nm thick HfO2 was used. In addition, gate metal, which has a work function of 4.54 eV and 4.8 eV, is used for nMOS and pMOS of CFET respectively.

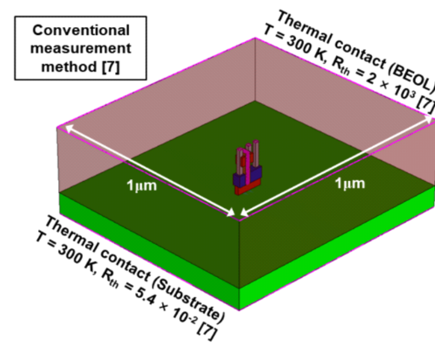

Fig.6 The 3-nm node CFET with boundary conditions.

Fig. 6 shows schematics of the thermal parameters used in TCAD. Thermal modeling is based on the simulation setup of the conventional model suggested by [12]–[19]. As shown in Fig. 6, the CFET locates on a wide silicon substrate and is surrounded by SiO2.Boundaries are then set on the top and bottom surfaces for realistic heat dissipation modeling [12].

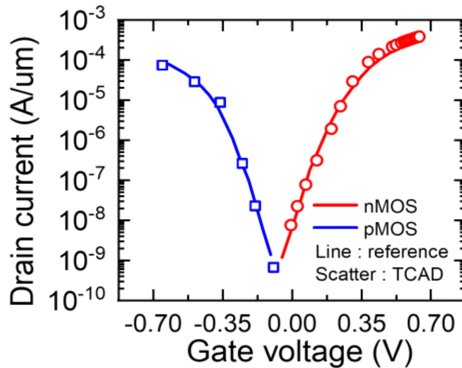

Fig.8 Calibrated transfer characteristics of CFET.

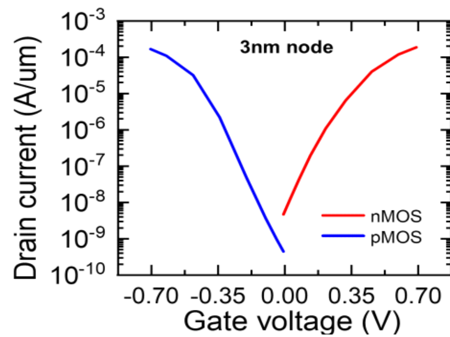

Fig.9 Transfer characteristic of CFET, for the 3-nm

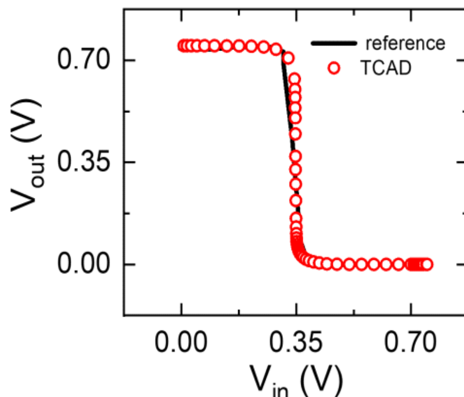

Fig.10 VTC of CFET

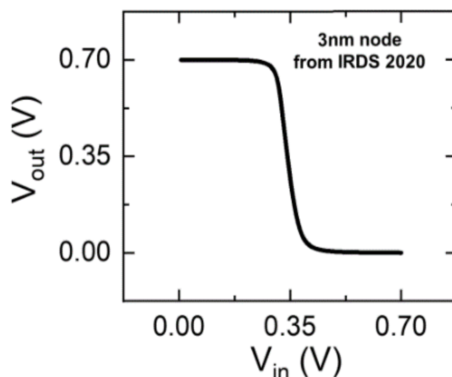

Fig.11 VTC of CFET for the 3-nm node

Fig. 8 shows the method of calibration of the TCAD to reference for realistic simulation. The calibration of TCAD is performed for the transfer characteristic and voltage transfer characteristic (VTC) of CFET (Fig. 8 and 10) from the experimental reference with a gate length of 75 nm [7].

This is the only fabricated CFET with vertically stacked NSHFETs that can operate as inverters with a high on state current and low SS. Then, a 3-nm node CFET is designed using the IRDS specifications, as shown in Table 1, and the DC performances and inverter performances.

For device physics, models of density gradient quantum correction and inversion accumulation mobility are used to consider quantum confinement in Nano scale devices.
In addition, bandgap narrowing, electric-field-dependent mobility, doping-dependent mobility, high field saturation, Shockley-Read-Hall doping dependence and band-to-band tunneling (Hurkx) were used. Parameters for respective physics are used from default value provided TCAD. The model was also applied to simulate realistic carrier transportation with the parameters listed in Table 2 [12]–[19].

The transient response of the 3-nm node CFET. The transient response of the 3-nm node CFET is calculated by ‘‘mixed-mode’’ of TCAD. The power supply voltage (Vdd) is set to 0.6 V . For the transient response, the inverter performance is calculated based on the fan-out of the 3 (FO3) logic inverter circuit. [20], [21].

Here, Ceff is calculated from the general equation
Ceff = total gate capacitance(Cgg) + total drain capacitance (Cdd) + 3 (number of fanout devices) × fan-out capacitance (Cfo) [20], [21].
Cfo is assumed to be the same as Cgg

Therefore

$$Ceff = 4 \times Cgg + Cdd.$$

Cgg and Cdd are extracted from a single CFET device.
Here, Cgg includes the gate-to-drain capacitance (Cgd), gate-to-source capacitance of nMOS (Cgsn), and gate to-source capacitance of pMOS (Cgsp). For the performance parameters, f is extracted using the equation shown in Fig.13.

Power is calculated using Ceff × f × V2dd,
PDP is calculated as power/f,
Reff is calculated as 1 / (Ceff ×f)[20], [21].

RESULTS AND DISCUSSION

To investigate the inverter performance characteristics, f , power, Ceff, and Reff of the 3-nm node CFET were compared for different structures and dimensions.f , PDP, Ceff, and Reff for different numbers of stacked channels of nMOS and pMOS(NnMOS, NpMOS) are compared. For NnMOS and NpMOS, NnMOS/NpMOS of 1/2, 2/3, 3/4, and 4/5 were used to compare inverter performances of the 3-nm node CFET for different NnMOS and NpMOS. For each device with NnMOS/NpMOS, the transfer characteristics of the nMOS and pMOS were calibrated to obtain the same VTC characteristics. NpMOS was chosen for a higher number than NnMOS to match the drain current, because the mobility of nMOS is much lower than that of pMOS. where f is calculated as 1 / (Reff × Ceff). The increment of NnMOS and NpMOS induces a higher drive current (Idrive) because of the large effective width and reduces Reff; however, Ceff increases as the gate area and height of the metal via increase. The device with NnMOS of 2 and NpMOS of 3 shows the highest f . PDP is calculated as Ceff × V^2dd in general; therefore, PDP is

proportional to Ceff [20], [21]. Thus, the increment in NnMOS and NpMOS triggers an increment in Ceff, so PDP increases.Ceff changes linearly by different dimensions, but Reff changes non-linearly. The reason of Reff's non-linearity is the impact of physics. Increment of current with increment of dimensions increases device temperature. The increased temperature degrades current and increases Reff.In f , PDP, Ceff, and Reff are compared for different values of Dnsh, Dn/p, Tnsh, and Wnsh. For Dnsh and Dn/p, ranges of 7–11 nm and 20–70 nm were used, respectively. In addition, Wnsh and Tnsh, ranging from 15 to 25 nm and 6 to 10 nm, respectively, were used. For Dnsh and Dn/p in increase in Dnsh and Dn/p can reduce f and increase PDP. The changes in Dnsh and Dn/p rarely cause a change in Reff as the effective width is constant and Idrive does not change. Therefore, Ceff dominantly determines f for the changes in Dnsh and Dn/p. Here, the reduction of both Dnsh and Dn/p triggers a low Ceff.

This is because the gate fringe electric field overlap is triggered between nMOS and pMOS of the CFET with a vertically stacked structure [4], [10]. In addition, the reduced height of the metal via decreases Ceff [10]. Thus, f increases with a reduction in Dnsh and Dn/p. Since PDP is proportional to Ceff, the reduction in Dnsh and Dn/p can decrease PDP with lower Ceff. The device with the optimum values for Tnsh of 9 nm and Wnsh of 21 nm . is required for the highest f .Thus, a higher effective width decreases Reff, and a larger gate area increases Ceff with increasing Tnsh and Wnsh. In addition, because of the increase in Ceff, PDP increases with increasing Tnsh and Wnsh.

CONCLUSION

3-D TCAD calibration, the inverter performance and thermal properties of a 3-nm node CFET with varying dimensions were examined for the first time. Furthermore, recommendations for CFET device design were made in order to improve the inverter's performance and thermal properties.First, inverter performances by different NnMOS, NpMOS, Dnsh, Dn/p, Tnsh, and Wnsh were investigated. For NnMOS and NpMOS, with a reduction in the above parameters, Ceff decreases because the gate area decreases and the height of the metal via is reduced. However, Reff increases with a decrease in the effective width. Therefore, an optimum NnMOS/NpMOS ratio of 2/3 is required for the highest f as a trade-off between Ceff and Reff. For Dnsh and Dn/p, their reduction decreases the height of the metal gate and source/drain metal via, thereby reducing Ceff without changing Reff. Thus, the reduction of Dnsh and Dn/p can increase f and decrease PDP. Subsequently, the thermal characteristics by different NnMOS, NpMOS, Dnsh, Dn/p, Tnsh, and Wnsh were investigated. For the different NnMOS and NpMOS, their reduction decreases the gate area and disturbs the heat dissipation from the devices to the thermal ground, thereby increasing Rth. In the case of Dnsh and Dn/p, their reduction induces a higher Rth because of severe thermal coupling, but the change in Rth is negligible. Considering both inverter accomplishment and thermal characteristics from the perspective of down-scaling, it is notable that the reduction in Dnsh and Dn/p of CFET can improve both f and PDP without severe degradation. This is different from the other dimension parameters; results demonstrate a significant trade-off between thermal parameters and inverter performance. This study can provide crucial insights into the device design of CFET for a sub-3-nm node.

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References

1. P. Weckx et al., "Novel forksheet device architecture as ultimate logic scaling device towards 2 nm," in IEDM Tech. Dig., Dec. 2019,pp. 871–874, doi: 10.1109/IEDM19573.2019.8993635.
2. J. Ryckaert et al., "The complementary FET (CFET) for CMOS scaling beyond N3," Proc. IEEE Symp. VLSI Technol., Jun. 2018, pp. 141–142, doi: 10.1109/VLSIT.2018.8510618.
3. S.-W. Chang et al., "First demonstration of CMOS inverter and 6T-SRAM based on GAA CFETs structure for 3D-IC applications,"in Proc. IEEE Int. Electron Devices Meeting (IEDM), 2019, pp. 11.7.1–11.7.4, doi: 10.1109/IEDM19573.2019.8993525.
4. S. Subramanian et al., "First monolithic integration of 3D complementary FET (CFET) on 300mm Wafers," in Proc. IEEE Symp. VLSI Technol., 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265073.
5. C.-Y. Huang et al., "3-D self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued Moore's Law scaling," in Proc. IEEE Int. Electron Devices Meeting (IEDM), 2020, pp. 20.6.1–20.6.4, doi: 10.1109/IEDM13553.2020.9372066.
6. M. G. Bardon et al., "Power-performance trade-offs for lateral nanosheets on ultra-scaled standard cells," in Proc. IEEE Symp. VLSI Technol., 2018, pp. 143–144, doi: 10.1109/VLSIT.2018.8510633.
7. D. Yakimets et al., "Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology," in Proc. IEEE Int. Electron Devices Meeting (IEDM), 2017, pp. 20.4.1–20.4.4, doi: 10.1109/IEDM.2017.8268429.
8. P. Schuddinck et al., "Device- circuit- & block-level evaluation of CFET in a 4 track library," in Proc. Symp. VLSI Technol., Jun. 2019, pp. T204–T205, doi: 10.23919/VLSIT.2019.8776513.
9. "International Roadmap for Devices and Systems (IRDSTM)." 2020. [Online]. Available: https://irds.ieee.org/editions/2020
10. T. Cui, Q. Xie, Y. Wang, S. Nazarian, and M. Pedram, "7nm FinFET standard cell layout characterization and power density prediction in near- and super-threshold voltage regimes," in Proc. Int. Green Comput. Conf., 2014, pp. 1–7, doi: 10.1109/IGCC.2014.7039170.
11. J. M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits: A Design Perspective. Englewood Cliffs, NJ, USA: Prentice Hall, 1996.
12. Y. Taur and T. H. Ning. Fundamentals of Modern VLSI Devices. Cambridge, U.K.: Cambridge Univ. Press, 2009.oi: 10.1109/IEDM19574.2021.9720601.
13. J. Ryckaert et al., "The Complementary FET (CFET) for CMOS scaling beyond N3," in Proc. IEEE Symp. VLSI Technol., Jun. 2018, pp. 141–142, doi: 10.1109/VLSIT.2018.8510618.
14. C.-Y. Huang et al., "3-D self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued Moore's law scaling," in IEEE Int. Electron Devices

Meeting Tech. Dig., Dec. 2020, pp. 20.6.1–20.6.4,doi: 10.1109/IEDM13553.2020.9372066.
15. S.-W. Chang et al., "First demonstration of CMOS inverter and 6T-SRAM based on GAA CFETs structure for 3D-IC applications," in IEEE Int. Electron Devices Meeting Tech. Dig., Dec. 2020, pp. 11.7.1–11.7.4, doi: 10.1109/IEDM19573.2019.8993525.
16. T.-Z. Hong et al., "First demonstration of heterogenous complementary FETs utilizing low-temperature (200◦C) hetero-layers bonding technique (LT-HBT)," in IEEE Int. Electron Devices Tech. Dig., Dec. 2020,pp. 15.5.1–15.5.4, doi: 10.1109/IEDM13553.2020.9372001.
17. Y.-J. Lee et al., "Low-temperature microwave annealing for MOSFETs with high-k/metal gate stacks," IEEE Electron Device Lett., vol. 34, no. 10, pp. 1286–1288, Oct. 2013, doi: 10.1109/LED.2013.2279396.
18. Sentaurus TCAD Version 2019, Synopsys, Mountain View, CA, USA, 2019.
19. R. Zhang, X. Yu, M. Takenaka, and S. Takagi, "Impact of channel orientation on electrical properties of Ge p- and n-MOSFETs with 1-nm EOT Al2O3/GeOx/Ge gate-stacks fabricated by plasma postoxidation," IEEE Trans. Electron Devices, vol. 61, no. 11, pp. 3668–3675, Nov. 2014, doi: 10.1109/TED.2014.2359678.
20. L. P. B. Lima, H. F. W. Dekkers, J. G. Lisoni, J. A. Diniz, S. Van Elshocht, and S. De Gendt, "Metal gate work function tuning by Al incorporation in TiN," J. Appl.
21. S. Subramanian et al., "First monolithic integration of 3D complementary FET (CFET) on 300mm wafers," in Proc. IEEE Symp. VLSI Technol., Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265073.

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