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Research Article

A SIMPLE SEPIC DERIVED DC-DC CONVERTER WITH TL494 PWM IC BASED CONTROLLER

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ABSTRACT

The Single-Ended Primary-Inductor Converter (SEPIC) is capable of operating from an input voltage that is greater or less than the regulated output voltage. It can function as both buck and boost converter, and has minimal active components. TL494 PWM controller is used to regulate the output voltage. The converter is designed for an input voltage variation of 40V- 60V and a regulated output voltage of 48V. Design of converter parameters, hardware implementation and results obtained are produced.

INTRODUCTION

DC-DC converters convert DC power to another DC level. By closed loop Pulse Width Modulation (PWM) of the gate signals (Kwasinski, 2009). Switching frequency of the gate signal, in most cases, is high (greater than 20 kHz) and constant. Figure 1 shows a block diagram of a DC-DC converter with closed loop control.

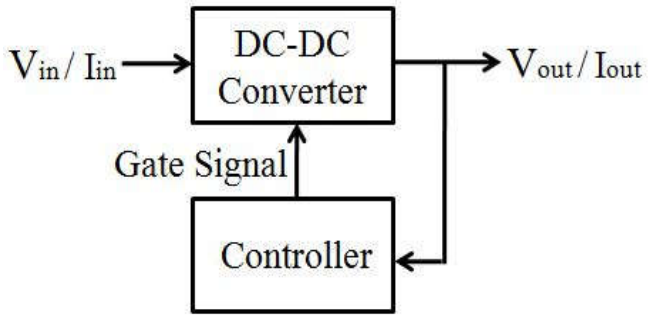

Figure 1 Block diagram of a DC-DC converter with closed loop control

DC-DC converters can be classified as non isolated DC-DC converters and isolated DC-DC converters (Yoshino. T, 2014). Six most popular topologies of non isolated classical type DC-DC converters are, Buck, Boost, Buck-Boost, Cuk, Zeta and SEPIC.

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SEPIC is capable of operating from an input voltage that is greater or less than the regulated output voltage (Sahoo. M and Kumar. K.S, 2014). It can function as both buck and boost converter with minimal active components. Its control system is simple, and had clamped switching waveforms that provide low noise operation (Robert Kollman, 2009). The SEPIC is often identified by its use of two magnetic windings. These windings can be wound on a common core, as in the case of a coupled dual winding inductor, or they can be the separate windings of two uncoupled inductors. In this paper, a novel single switch SEPIC DC-DC converter with low voltage stress on the power switch is proposed (Texas Instruments,2003). The structure of the proposed converter is simple, hence the control of the converter will be easy (Texas Instruments, 2014). The voltage stress across the power switch and diodes is less than the output voltage, hence the conduction loss of the power switch is low and the efficiency of the presented converter is more (Robert Kollman, 2009). The presented converter operates as a universal power supply and it is appropriate for low voltage and low power applications. The proposed SEPIC converter finds application in fuel cell systems, car electronic devices, LED drivers, and gadgets, such as mobile phones and notebooks.

Operating Principle

The SEPIC converter (Abraham I Pressman, 1991) shown in Figure.2, uses two inductors: L_1 and L_2. The two inductors can be wound on the same core since the same voltages are applied to them throughout the switching cycle. This converter has one

power switch Q_1, diode D_1, two inductors L_1 and L_2, three capacitors C_{in}, C_s, and C_{out} and load R. For simplicity the input and output capacitors are assumed to be large enough to avoid, voltage ripples. The main switch of the proposed converter is treated as ideal. (M.H. Rashid, 1988) The proposed converter can be operated in both the Continuous Conduction Mode (CCM) and the Discontinuous Conduction Mode (DCM). The CCM can be divided into two:

In First mode as in Figure 2(a) the switch Q_1 is turned ON and the diode D_1 is reverse biased. The inductors L_1, L_2 gets charged. The capacitors C_s is discharged through L_2. Output is delivered by the capacitor C_{out}.

During mode 2, the switch Q_1 is turned OFF and the diodes D_1 is turned ON as shown in Figure 2(b). The inductors L_1, L_2 are discharged linearly. The capacitor C_s is charged by the inductor L_1 and the capacitor C_{out} is charged by the inductors L_1 and L_2. Output current is the sum of both inductor currents.

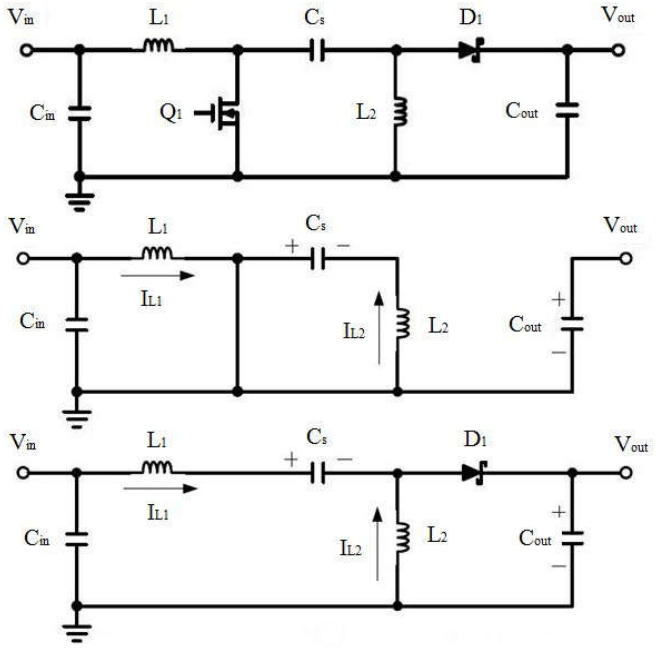

Figure 2 SEPIC Converter Current Flow (a) During Q_1 On-Time, (b) During Q_1 Off-Time.

Waveforms During CCM

During steady state CCM neglecting ripple voltage, capacitor C_s is charged to the input voltage, V_{in}. Voltage waveforms are shown in Figure 3. When Q_1 is OFF, the voltage across L_1 is V_{out}. Since C_{in} is charged to V_{in}, the voltage across Q_1 when Q_1 is OFF is $V_{in} + V_{out}$, so the voltage across L_1 is V_{out} (Texas Instruments, 2003). When Q_1 is ON, capacitor C_s, is charged to V_{in} and is connected in parallel with L_2 , so that the voltage across L_2 is V_{in}.

The currents flowing through switch Q_1, diode D_1, capacitor C_1 and inductors L_1, L_2 are shown in Figure 4. When Q_1 is ON, energy is being stored in L_1 from the input and in L_2 from C_s. When Q_1 turns OFF, current through L_1 continues to flow through C_s and D_1, and also through C_{out} and the load. Both C_{out} and C_s get recharged so that they can provide the load current and charge L_2, respectively, when Q_1 gets ON.

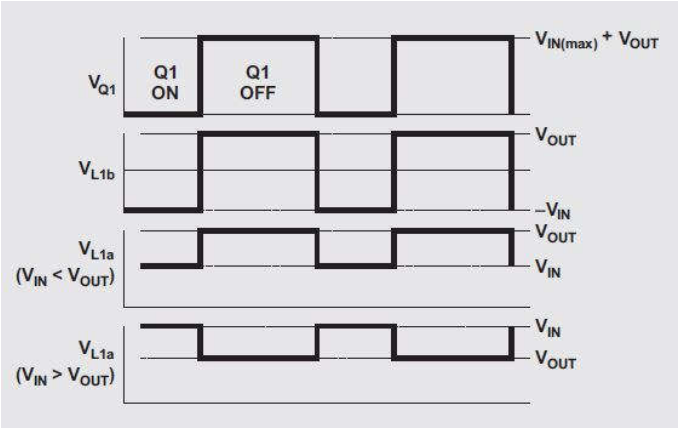

Figure 3 SEPIC voltages during CCM

Figure.5 shows the capacitor ripple voltage as related to the output capacitor current. When Q_1 is ON, the output capacitor must provide the load current. Therefore, the output capacitor must have at least enough capacitance, but not too much ESR, to meet the applications requirement for output voltage ripple, V_{RPL}. Thus for a SEPIC converter operating in CCM, the duty cycle is given by:

$$D = \frac{V_{out} + V_D}{V_D + V_{in} + V_{out}}$$

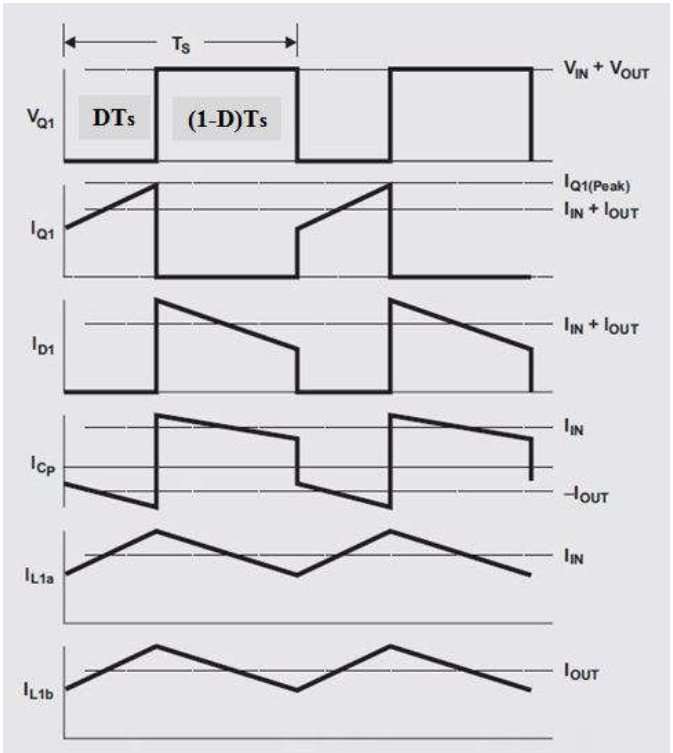

Figure 4 SEPIC component currents during CCM

V_D is the forward voltage drop of the diode D_1. The maximum duty cycle is:

$$D_{max} = \frac{V_{out} + V_D}{V_D + V_{in,min} + V_{out}}$$

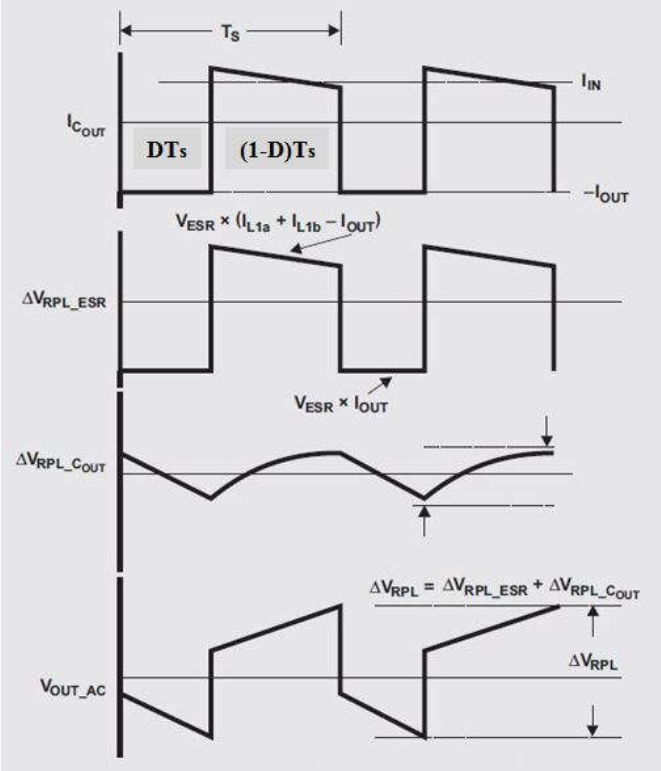

Figure 5 Ripple voltage of output capacitor

The TL494 PWM Controller

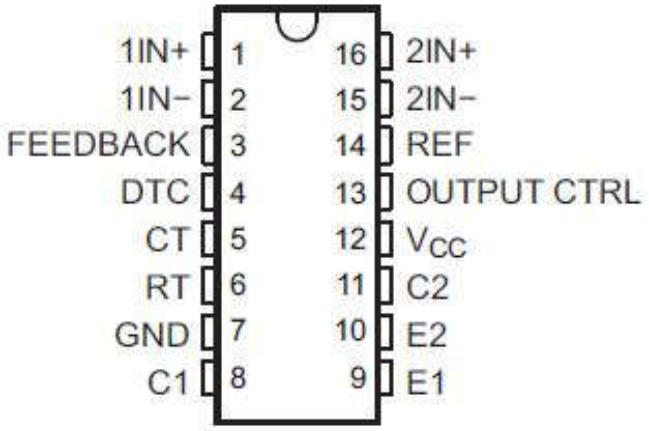

Figure 6 TL494 PWM IC

The TL494 is one of the earliest PWM controllers used in Switched Mode Power Supplies (SMPS's). It incorporates all the functions required in the construction of a PWM control circuit on a single chip. Designed primarily for power supply control, this device offers the flexibility to tailor the power supply control circuitry to a specific application.

The design of the TL494 (Texas Instruments, 2017) not only incorporates the primary building blocks required to control a switching power supply, but also addresses many basic problems and reduces the amount of additional circuitry required in the total design. Figure.7 gives block diagram of the TL494.

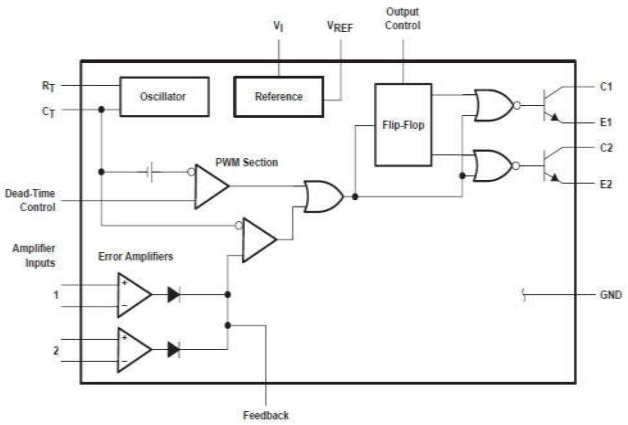

Figure 7 Block diagram of the TL494

The TL494 is a fixed frequency PWM control circuit. Modulation of output pulses is accomplished by comparing the saw tooth waveform created by the internal oscillator on the timing capacitor to either of two control signals Q_1 and Q_2. The output stage is enabled during the time when the sawtooth voltage is greater than the voltage control signals. As the control signal increases, the time during which the sawtooth input becomes greater decreases; therefore, the output pulse duration decreases. A pulse steering flip flop alternately directs the modulated pulse to each of the two output transistors. Figure 8 shows the relationship between the pulses and the signals.

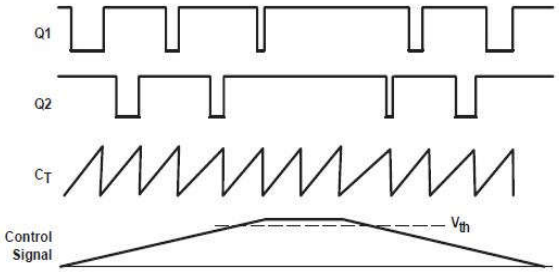

Figure 8 Relationship between the pulses and the signals.

The control signals are derived from dead time (OFF-time) control circuit and the error amplifier. The dead time control input is compared directly by the dead time control comparator. This comparator has a fixed 100mV offset. With the control input biased to ground, the output is inhibited during the time that the sawtooth waveform is below 110 mV. This provides a preset dead time of approximately 3 percentage, which is the minimum dead time that can be programmed. The PWM comparator compares the control signal created by the error amplifiers. One function of the error amplifier is to monitor the output voltage and provide sufficient gain so that millivolts of error at its input, result in a control signal of sufficient amplitude to provide 100 percentage modulation control. The error amplifiers also can be used to monitor the output current and provide current limiting to the load.

5 V Reference Regulator

The TL494 internal 5 V reference regulator can provide a stable reference, and will act as a pre-regulator. It can establish a stable supply from which the output control logic, pulse steering flip flop, oscillator, dead time control comparator, and PWM comparator are powered. The reference is internally programmed to an initial accuracy of 5 percentage and

maintains a stability of less than 25mV variation over an input voltage range of 7 V to 40 V. For input voltages less than 7 V, the regulator saturates within 1 V of the input and tracks it.

Comparator

The comparator is biased from the 5V reference regulator. This provides isolation from the input supply for improved stability. The input of the comparator does not exhibit hysteresis, so protection against false triggering near the threshold must be provided. The comparator has a response time of 400ns from either of the control signal inputs to the output transistors, with only 100 mV of overdrive. This ensures positive control of the output within one half cycle for operation within the recommended 300 kHz range.

Pulse Width Modulation (PWM)

The comparator also provides modulation control of the output pulse width. For this, the ramp voltage across timing capacitor C_T is compared to the control signal present at the output of the error amplifiers. The timing capacitor input incorporates a series diode that is omitted from the control signal input. This requires the control signal (error amplifier output) to be 0.7 V greater than the voltage across C_T to inhibit the output logic, and ensures maximum duty cycle operation without requiring the control voltage to sink to a true ground potential. The output pulse width varies from 97 percentage of the period to '0 ' as the voltage present at the error amplifier output varies from 0.5 V to 3.5 V, respectively.

Oscillator

The oscillator provides a positive sawtooth waveform to the dead time and PWM comparators for comparison to the various control signals. The frequency of the oscillator is programmed by selecting timing components R_T and C_T .The oscillator charges the external timing capacitor, C_T , with a constant current; the value of which is determined by the external timing resistor, R_T . This produces a linear ramp voltage waveform. When the voltage across C_T reaches 3 V, the oscillator circuit discharges it and the charging cycle is reinitiated. The frequency of the oscillator becomes,

$$f_{osc} = \frac{1}{R_T C_T}$$

The oscillator is programmable over a range of 1 kHz to 300 kHz. Practical values for R_T and C_T range from 1 k to 500 k and 470 pF to 10 F, respectively. A plot of the oscillator frequency versus R_T and C_T is shown in Figure 9.

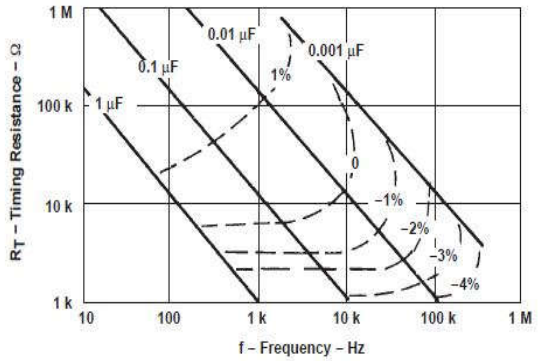

Figure 9 Switching frequency selection graph

Design of Proposed Sepic Converter

User Specifications

Minimum input voltage V_{dcmin} = 40V
Maximum input voltage V_{dcmax} = 60V
Output ripple voltage = 50 mV
Output voltage V_o = +48V
Maximum load current I_o = 1:5A
Maximum output power P_o = 72W

Designer Specifications

Switching frequency f_{SW} = 100kHz

Switch Specifications

Switch selected is the N Channel enhancement type MOSFET 10N100E
V_{DSmax} = 1000V
I_{DSmax} = 10A
t_r = 40 ns
t_f = 40 ns
R_{dsON} = 1.9
Q_{gtotal} = 34 nC
V_{GS} = 10V

Duty cycle calculation

For a SEPIC converter operating in a CCM, the duty cycle is given by:

$$D_{min} = \frac{V_{out} + V_D}{V_D + V_{in,max} + V_{out}}$$

$$D_{max} = \frac{V_{out} + V_D}{V_D + V_{in,min} + V_{out}}$$

Assume that the V_D is 0.5 V. Therefore,

D_{min} = 0.334
D_{max} = 0.448

Inductor Selection

A good rule for determining the inductance is to allow the peak to peak ripple current to be approximately 40 percentage of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L_1 and L_2 is given by:

$$I_L = \frac{I_{out} * V_{out} * 40}{V_{in,min} * 100}$$

$$I_L = \frac{1.5 * 48 * 40}{40 * 100}$$

$$I_L = 0.72 \text{ A}$$

and the inductance for L_1 and L_2 is:

$$L_1 = L_2 = \frac{V_{in,min} * D_{max}}{I_L * f_{sw}}$$

Where f_{sw} is the switching frequency and D_{max} is the duty cycle at the minimum V_{in}.

$$L_1 = L_2 = \frac{40 * 0.548}{0.72 * 100 * 1000}$$

$$L_1 = L_2 = 304.44 \text{ uH}$$

The peak input inductor current is:

$$I_{L1,peak} = \frac{I_{out} * (V_{out} + V_D) * (2 + .04)}{V_{in,min} * 2}$$

$$I_{L1,peak} = 2.1825 \text{ A}$$

$$I_{L2,peak} = \frac{I_{out} * (2 + .04)}{2}$$

$$I_{L2,peak} = 1.8 \text{ A}$$

Output Diode Selection

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current $I_{Q1;peak}$. The minimum peak reverse voltage the diode must withstand is:

$$V_{RD1} = V_{in,min} + V_{out,max}$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended in order to minimize the efficiency loss.

SEPIC Coupling Capacitor Selection

The selection of SEPIC capacitor, C_s, depends on the RMS current, which is given by:

$$I_{cs,rms} = \frac{I_{out} * \sqrt{V_{out} + V_D}}{\sqrt{V_{in,min}}}$$

$$I_{cs,rms} = \frac{1.5 * \sqrt{48 + 0.5}}{\sqrt{40}}$$

$$I_{cs,rms} = 1.1\ A$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for coupling capacitor, having high RMS current ratings relative to size. Electrolytic capacitors work well for through hole applications where the size is not limited and they can accommodate the required RMS current rating.

The peak to peak ripple voltage on C_s (assuming no ESR):

$$V_{Cs} = \frac{I_{out} * D_{max}}{C_s * f_{sw}}$$

$$V_{Cs} = \frac{2 * 0.448}{C_s * 300 * 1000} = 0.42\ V$$

A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on Cs. Hence, the peak voltage is typically close to the input voltage. Thus Cs is selected as

$C_s = 10\ \mu F$
Not only that,
$C_{in} = 500\ \mu F$
$C_{out} = 2200\ \mu F$

Scheme of the DC-DC Converter Using Sepic Topology

The proposed scheme has three sections, the supply part, converter part and load. SEPIC converter is used to convert unregulated DC supply input to regulated DC supply output. This converter is fed from a 40 - 60 V supply and the output voltage of 48 V is fed to a resistive load. The circuit is designed for 1.5A current rating. For the generation of gating pulses TL494 PWM controller is used, which regulates the output voltage to the required value for any supply or load variations. For that 48V output which is stepped down into 5V, is continuously compared with the reference 5V using a feedback arrangement. PWM signals are generated based on error voltage. These pulses are given to the MOSFET.

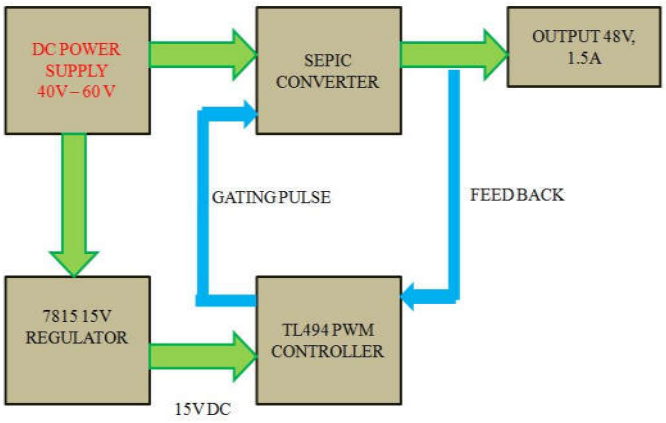

Figure 10 Scheme of the DC-DC converter using SEPIC Topology

Main advantage of this scheme is that we can have wider input and output ranges. Also the whole system is small in size because of the PWM IC and high frequency converter, say 100 kHz.

Proposed Circuit Diagram

40- 60 V DC power supply is the input to the converter, and input to the driver IC is 15 V (15 V and 5V are generated from the supply input). TL494 need separate power supply of input 9 V (fed from a 9V DC adapter).

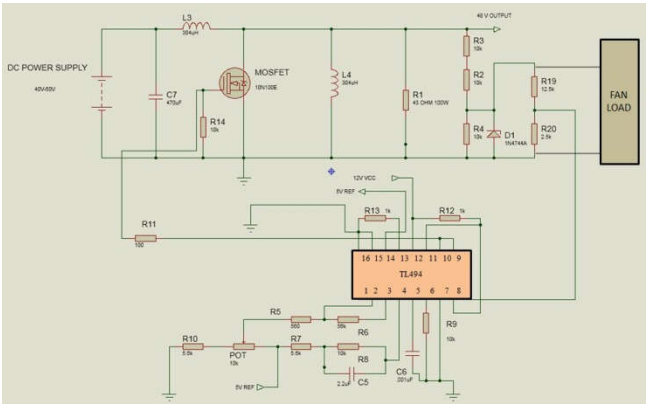

Figure 11 Circuit Diagram of the proposed DC-DC Converter Closed loop

SIMULATION RESULTS

To verify the feasibility and validity of the proposed converter, MATLAB software version 16 (MATLAB SIMULINK 2016) is used for the simulation.

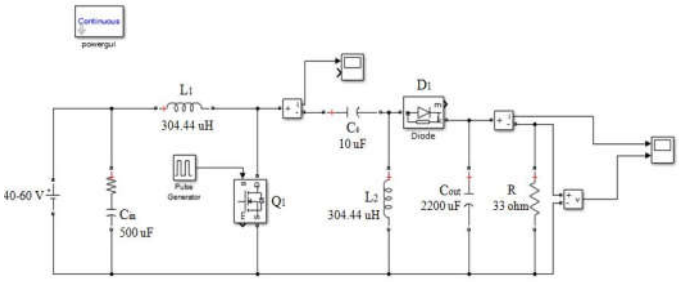

Figure 12 Simulink open loop Model

The output waveforms are shown in Figure.13 and Figure.14. The converter is operated in both buck and boost mode. For an input of 40 - 60 volts and output voltage is 48 volts. The

switch is controlled by a pulse generator with a duty ratio of .448 - .334 and at a switching frequency of 100KHz.

Thus for varied input voltage 40 - 60 V constant output voltage is obtained by varying the duty ratio from minimum to maximum value in the SEPIC converter in open loop simulation. Now the SEPIC converter can be in closed loop by resistor divider arrangement at the output resistance for voltage feedback. The output waveforms shows that a 48 V constant output voltage is obtained with an output current of 1.18 A.

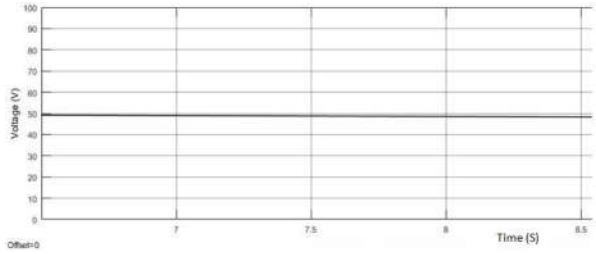

Figure 13 Output voltage waveform

Figure 14 Output current waveform

EXPERIMENTAL RESULTS

The hardware prototype is soldered on a dotted PCB including the gate driver circuit. Heat sinks are mounted for switch, diodes and voltage regulators. Heat sink compound is applied for maximum heat conduction and electrical isolation. In addition a small cooling fan is mounted for cooling the MOSFET.

Hardware Setup

The component ratings under transient and steady state are obtained from design and simulation results. The component ratings are chosen as considering voltage rating, current rating, availability and cost, MOSFET switch 10N100E has been selected. Its specifications include collector to emitter voltage of 1000V and collector current 10A. The switch can operate at a switching frequency of 200 kHz. To trigger the switch a TL494 PWM IC is required. The PWM IC is to be designed to generate switching signals at required duty ratio and frequency.

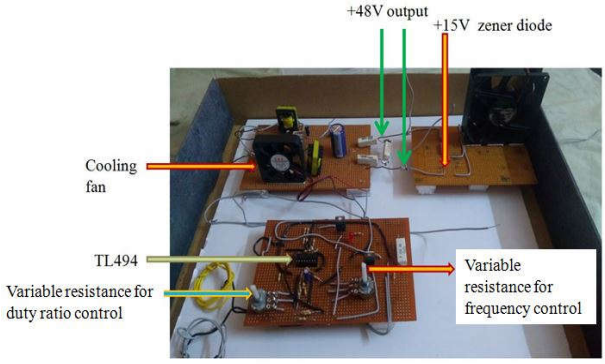

Figure 15 Hardware set up

PWM pulse generation

Primary aim is to generate the PWM signal of the required pulse width and frequency. Figure.16 shows the test setup for the generation of the PWM pulses. The TL494 PWM IC requires 12V for its operation then an internal 5V is generated and can be used as the reference voltage. An external DC supply of 5 V is used as the feedback voltage.

When supply is switched ON PWM pulses are generated as shown in Figure.17 and with the help of potentiometer arrangement we can adjust frequency and duty ratio of pulses to required value. It is observed that when the feedback voltage is more than the reference voltage the IC stops pulse generation and the converter does not work.

Figure 16 PWM pulse generation

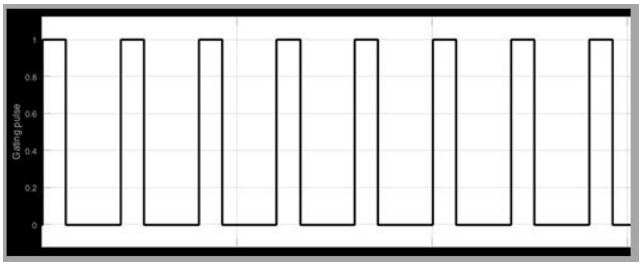

Figure 17 Gating pulse for the SEPIC Converter

Testing of the complete circuit

After the verification of the PWM pulses the next step is to test the complete circuit, that is TL494 PWM IC working along with the SEPIC converter. This final testing is important for the overall success of the SMPS.

Testing of the system requires two power supplies, 40-60 V variable power supply for the input of the SMPS (two 0-30 V, 5 A power supplies are connected in series is used)and 9 V power supply for the operation of TL494 PWM IC (9 V,1 A DC adapter is used).

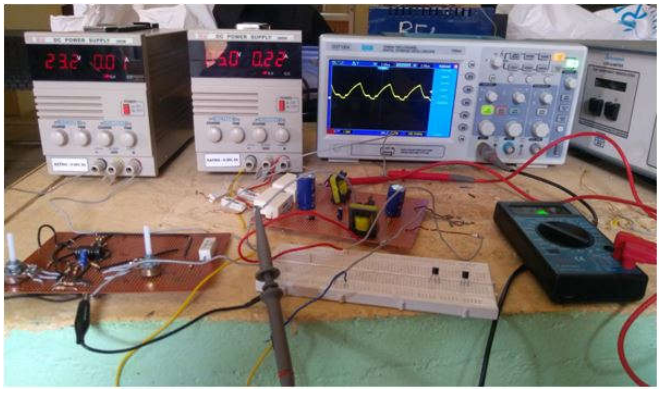

Figure.18 Line Regulation Test at 40V

From the test, when minimum DC voltage (40 V) is applied an output of 48V is generated. During line regulation test when the input voltage increases to 60 V the output does not change. This is due to the use of coupled inductor. Also it can see that when the input voltage keeps on increasing the pulse width generated from the PWM IC keeps on decreasing. When the input DC voltage becomes more the limited value PWM IC stops generating PWM pulses and converter stops working.
Also the load test is conducted up to 50 percentage of rated load, it is observed that the 48 V output keeps on constant against the load variation. Overall the converter works on the expected level in the output side.

Line regulation (Output- 48 V)

For an input voltage of 40 - 60V, we have an output ranging from 48 - 48.19 V showing a good line regulation. A line regulation curve is drawn in Figure.19 based on Table 1. The Figure.20 shows the output wave form of the converter and its ripple content.

Table 1 Output voltage for different input voltage to draw the line regulation curve

INPUT DC VOLTAGE V_{dc} (V)	OUTPUT VOLTAGE V_{om} (V)
40	48.00
42	48.02
44	48.03
46	48.05
48	48.07
50	48.10
52	48.12
54	48.13
56	48.14
58	48.16
60	48.19

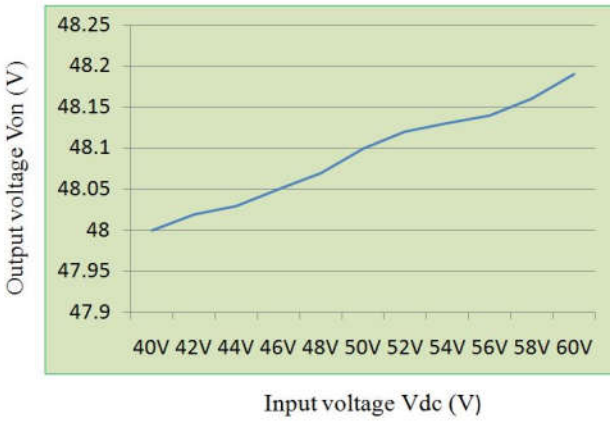

Figure.19 Line Regulation Curve

Figure.20 shows the output waveforms observed in the DSO. Output voltage is of good in quality and it is suitable for sensitive loads.

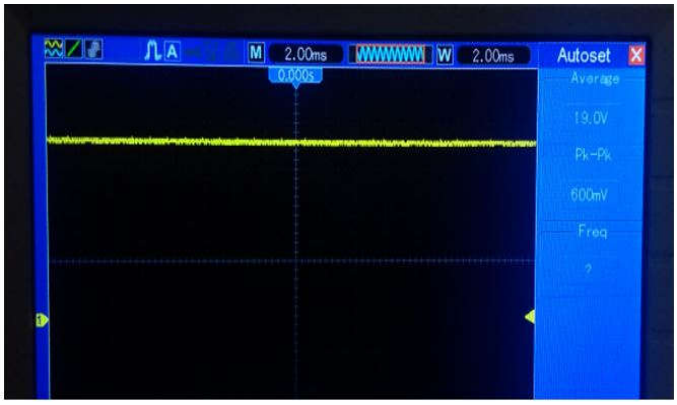

Figure 20 Output waveforms

CONCLUSION

Overall, the converter is good for wide input range applications, and is cost effective. An efficient 72 W SEPIC converter power supply is implemented utilizing TL494 PWM controller. The line regulation test reveals that the converter is capable of supplying constant 48 V DC output for input voltage variations of 40 V to 60 V DC. The load regulation test shows 50 percentage over load current without changing the output voltage. Output voltage contains lower amount of ripples and is non inverted which highlights the suitability for power supply applications. If coupled inductor type SEPIC converter will reduce the limitations of two separate inductor type SEPIC converter. The use of only one main switch decreases the conduction loss and improves efficiency with a wider operating range.

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